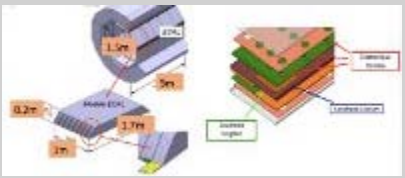
ECal: a piece of the jigsaw reaches a milestone

Hundreds of millions of channels of electronics: this is about what the electromagnetic calorimeter (ECal) of the CALICE collaboration will have to design, process and analyse. The very high granularity of ILC detector's future calorimeter will also be reflected in the ambitious first-stage electronics – or very-front-end electronics, which still needs to be designed. One part of the electronic jigsaw is the analogue-to-digital converter (ADC). At LPC, a CNRS/IN2P3 lab in Clermont-Ferrand, France, the latest ADC prototype fulfills the ILC requirements in terms of resolution, compactness, time of conversion and power consumption.

Each CALICE ECAL module is made of a heavy assembly of tungsten, silicon and electronics layers. At this level of miniaturisation these embedded electronics are better called "microelectronics". One of the key issues is their power consumption which should stay as low as possible with no possibility of cooling, at the order of 25 microwatts by channel. Another issue is integration: the readout electronics have to fit in a volume that must be as small as possible. Why such compactness? "We need an embedded ADC because of the type of calorimeter we want to build – it will be unprecedented in its granularity," said Laurent Royer, one of the engineers in charge of this study at LPC. "With external readout electronics, the ECAL would require too many wires and connectors and would have a very high power consumption. Therefore we could never afford to process so many electronics channels."



The CALICE electromagnetic calorimeter is a sandwich structure of thin wafers of silicon diodes, tungsten and front-end electronics layers (graphic: Marc Anduze, LLR)

In collaboration with LAL, Orsay, LPC jointly designed a chip to integrate a complete measurement system for the numerous required channels. The LPC electronics engineers conducting these studies, Laurent Royer and Samuel Manen, specialise in analogue and mixed systems such as analogue-to-digital converters. They had already designed and tested three prototypes of the ADC, with three types of architectures. The performance of these ADCs was evaluated with a dedicated high-precision test bench designed at Clermont-Ferrand. To characterise their chip, they first had to produce an analogue signal at the entrance of the ADC which precision was of course much higher than the one they aim for the ADC.

The generic motherboard designed at LPC to test the analogue-to-digital converter. Left with and right without ADC prototype.

The performance of LPC last prototype – a "12-bit cyclic architecture," is well adapted to future ECal in an ILC detector. Its resolution is 12 bits, which is equivalent to 500 microvolts for an input signal of 2 volts. The power consumption they obtained is under 0.5 microwatts per channel – for the ADC only, with the implementation of the required power pulsing system. Finally, this ADC is currently the one that fits the best the high ILC requirements in terms of consumption, linearity and precision.

The ADC team will go on with improving the reliability and the yield of their prototype. They will also test it together with the whole chain of the very-front-end in a multi-channels readout chip. The road is still long when the final technology chip will be sealed to the final ECal layer. But a good candidate for one piece of the big jigsaw is now ready.

-- Perrine Royole-Degieux

Read also the LPC team's talk at LCWS08 meeting